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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,540	11/21/2003	Shinichi Murakawa	245903US-2 CONT	7978
22850	7590	12/15/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			LEWIS, DAVID LEE	
			ART UNIT	PAPER NUMBER
			2673	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/717,540

Applicant(s)

MURAKAWA ET AL.

Examiner

David L. Lewis

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/21/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States.

1. Claims 21-25 are rejected under 35 U.S.C. 102(d) as being barred by applicant's Japan Patent filing, JP 2000-055964, Murakawa et al., published on 2/25/2000, and filed on 8/10/1998. Applicant has 1 year from the time of filing the foreign application (8/10/1998), to file the same invention in the United States or the patent is barred under 102(d).

As in Claim 21, Murakawa et al. teaches of an apparatus for testing a pixel electrode structure in which a plurality of pixel electrodes are arranged in a matrix of n rows and m columns, each of n and m being a natural number more than 1, and each of said plurality of pixel electrodes being activated, figures 1-7

comprising: a testing unit which has at least one potential sensor using an FET function in which a specific one of said plurality of pixel electrodes is used as a gate of an FET, figure 1 item 101;

Art Unit: 2673

wherein said at least one potential sensor is arranged opposite to said specific pixel electrode while keeping a predetermined distance from said specific pixel electrode, **figure 1 item d**

said potential sensor including two semiconductor regions of a first conductive type provided separately in a semiconductor region of a second conductive type, said FET function is realized by said potential sensor and said specific pixel electrode, **figure 5 item 207**

said potential sensor is activated in response to a sensor activation signal to output a voltage detection result associated with an activated pixel electrode, **figure 1 item 115;**

a drive section which relatively drives said testing unit to said specific pixel electrode with respect to said pixel electrode structure while keeping said predetermined distance, in response to a testing unit drive signal, **figure 1 item 105;**

and a control unit which outputs said testing unit drive signal to said drive section, sequentially activates said specific pixel electrode and pixel electrodes adjacent to said specific pixel electrode when said testing unit is driven to said specific pixel electrode, outputs said sensor activation signal to said testing unit, **figure 1 item 107,**

Art Unit: 2673

and detects a disconnection of said specific pixel electrode and a short-circuit between said specific pixel electrode and each of said adjacent pixel electrodes based on said voltage detection result, **figure 1 item 107, figure 4 items a and b.**

As in Claim 22, Murakawa et al. teaches of wherein said testing unit comprises: a plurality of said potential sensors arranged in one line, said control unit outputs said sensor activation signal to said testing unit for each of said plurality of potential sensors, **figure 2a item 207 (1N)**, sequentially activates ones of said plurality of pixel electrodes corresponding to said plurality of potential sensors when each of said plurality of potential sensors is activated, and detects the disconnections of said pixel electrodes corresponding to said plurality of potential sensors based on said voltage detection results from said testing unit, **figure 6 item 207.**

As in Claim 23, Murakawa et al. teaches of wherein when each of said plurality of potential sensors is activated, said control unit sequentially activates each of said adjacent pixel electrodes to said specific pixel electrode corresponding to the activated potential sensor, **figure 2a item 101/207 - c**, and detects the short-circuit between said specific pixel electrode and the activated adjacent pixel electrode based on said voltage detection result from said testing unit, **figure 1 item 107.**

As in Claim 24, Murakawa et al. teaches of wherein said testing unit comprises: said plurality of potential sensors, **figure 2a item 207**, a plurality of amplifiers respectively

Art Unit: 2673

connected with said plurality of potential sensors, **figure 2a item 209 (3N)**; and a scanner which sequentially selects outputs of said plurality of amplifiers for output to said control unit as said voltage detection result, **figure 2a item 211**.

As in Claim 25, Murakawa et al. teaches of wherein said testing unit comprises: said plurality of potential sensors, **figure 2a item 207**; a plurality of amplifiers respectively connected with said plurality of potential sensors, **figure 2a item 209**; and a scanner which sequentially selects outputs of said plurality of amplifiers for output to said control unit as said voltage detection result, **figure 2a item 211**.


Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis
December 11, 2005



BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
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